REMARKS

Claims 1-36 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. patent no. 5, 820,459 to Acres et al., which discloses a system and method for operating a plurality of gaming machines 22, 24, 26 connected to an associated floor controller 28 over a network. The floor controller can be connected to a series of microcontrollers in a daisy chain configuration shown in Fig. 12, wherein each microcontroller 248A-248H is, in turn, connected to a plurality of gaming machines over current loop networks, wherein each microcontroller can support two current loop networks, wherein each such current loop network can support up to 64 gaming machines (see column 19, lines 11-21 and 41-42).

The present invention differs fundamentally from the Acres et al. system in that it is directed to a system of a plurality of devices communicating with a host controller through a plurality of local controllers or nodes, wherein the devices may be located in a single gaming machine (see claim 12). In other words, the devices being controlled are not gaming machines themselves, but parts of gaming machines, such as individual switches, lights and the like. This is fundamentally different from the arrangement of Acres et al.

This difference is spelled out in the specific limitations of the independent claims of the subject application. Each of independent claims 1 and 5 specifies a gaming system comprising a plurality of devices to be individually accessed, a host controller and a plurality of local controllers interconnected with the host controller in a string, wherein each controller has a "power terminal" and a "common terminal," and further including a "power line interconnecting the power terminals of the host controller and all of the local controllers" and "a common line interconnecting the common terminals of the host controller and all of the local controllers." Claim 31, similarly recites a method of individually accessing a plurality of devices in a gaming system including local controllers and a host controller and including "providing a power line

connected to all of the controllers and a common line connected to all of the controllers." No such arrangement is disclosed or suggested by Acres et al.

The elements of the Acres et al. system are interconnected over an industry standard Ethernet network (column 7, lines 45-49). An Ethernet network does not supply power and ground to the devices on the network. Nor is there any need to provide power or ground to the controlled devices of the Acres et al. network, since the devices are gaming machines, each of which will be powered locally. The provision of power and ground connections to each of the accessed devices in the claimed invention however, is important, since these devices may be devices such as switches or lamps within an individual gaming machine.

Accordingly, it is believed that each of claims 1, 5, and 31 and the claims dependent thereon are patentable over Acres et al.

Each of independent claims 1, 5, 13, 24 and 31 also recites a gaming system wherein each of the local controllers has plural "device terminals" or "device output terminals" to which the individual control devices are "respectively connected." No such arrangement is disclosed or suggested by Acres et al. The examiner analogizes the claimed nodes or local controllers to the microprocessors 248A-248H of the Acres et al. floor controller (Fig. 12). But each Acres et al. microprocessor has two serial signal lines 251 which are, respectively, coupled to current loop networks through a current loop driver, each such current loop network in turn including a plurality of controlled gaming machines. The microprocessors 248A-248H do not have individual device terminals respectively connected to the controlled gaming machines. Thus, this is an additional reason why each of the independent claims and the claims dependent thereon patentably distinguishes from Acres et al.

Each of independent claims 13 and 24 further specifies, and claim 31 is amended herein to specify, that each node or local controller includes a "M-bit shift register" with the register positions "respectively connected" to "device output terminals," or "device terminals" and that the local controllers or nodes are interconnected so as to cooperate to provide "a (MxN)-bit shift register," the host controller producing a serial digital data stream "including MxN bits" respectively corresponding to the devices being controlled. No such arrangement is disclosed or suggested by Acres et al. In the Acres et al. arrangement, an individual microprocessor 248 does not form an M-bit shift register with positions respectively connected to the associated devices controlled by the microprocessor, nor do the group of microprocessors 248A-248H form a MxN-bit shift register. This affords an additional reason for allowance of the independent claims and the claims dependent thereon.

For all the foregoing reasons, it is submitted that each of claims 1-36, as amended herein, clearly distinguishes from Acres et al. and, accordingly, it is respectfully requested that the rejection of the claims be reconsidered and withdrawn and that the application be allowed.

Respectfully submitted,

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